AN3320K, AN3320S

VTR Playback Video Signal Processing Circuits

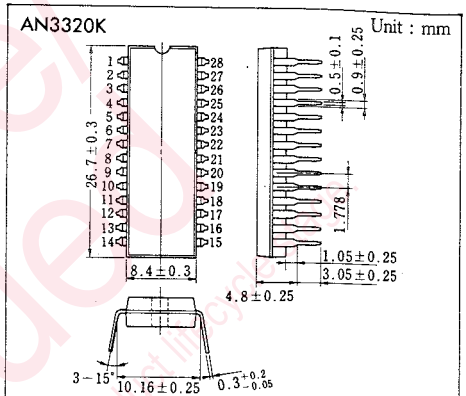
■ Outline

The AN3320K and the AN3320S are integrated circuits designed for VTR playback video signal processing circuits.

■ Features

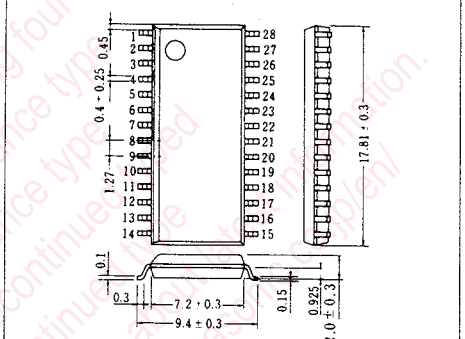
- Built-in line noise canceler
- Built-in picture control circuit
- Supply voltage : V_{CC}=5V

AN3320K Unit : mm



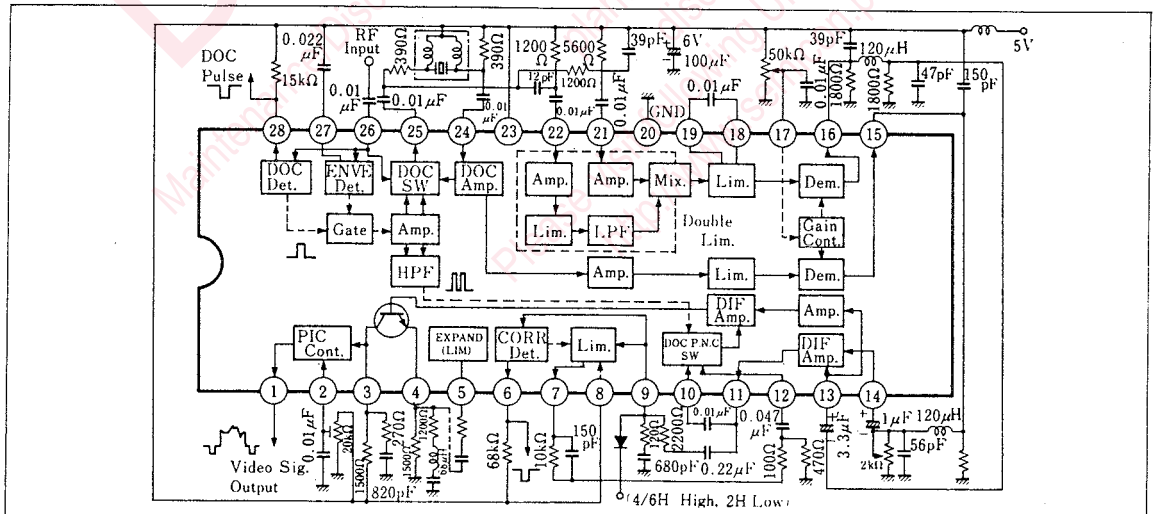
28-Lead Shrunk DIL Plastic Package

AN3320S Unit : mm



28-Lead PANAFLAT Package (SO-28D)

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25℃)

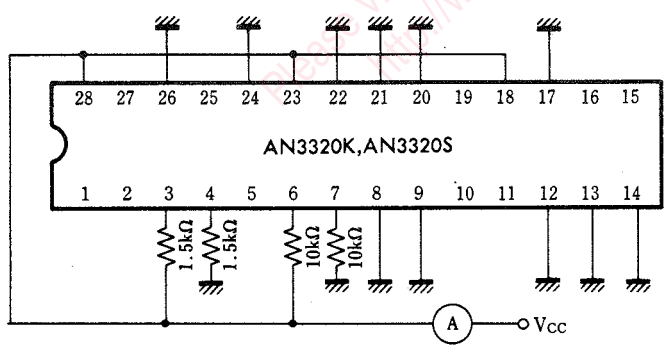
Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	6.0	V
Power Dissipation(Ta=70℃)	P_D	200	mW
Operating Ambient Temperature	T_{opr}	−20~+70	℃
Storage Temperature	T_{stg}	−55~+150	℃

■ Electrical Characteristics (V_{CC}=5V, Ta=25℃)

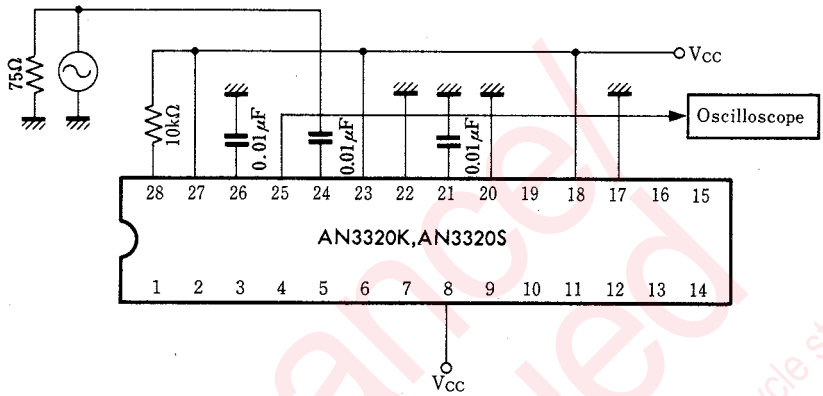
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit Current	I_{23}	1		17		30	mA
DOC Ampl. Gain	G_{25}	2	Pin ㉔ Input (60mV$_{P-P}$, 4MHz)	13		16	dB
DOC Sensitivity ON	S_{28}	3	Pin ㉖ Input (4MHz), 0 dB=350mV$_{P-P}$	−15		−11.5	dB
DOC Sensitivity OFF(Hystersis)	ΔS_{28}	3	Pin ㉖ Input (4MHz), 0 dB=350mV$_{P-P}$	−5		−0.5	dB
Sub FM Demodulation Det. Sensitivity	S_{15}	4	Pin ㉔ Input (50mV$_{P-P}$) ⑰ 3.5V F_{11} is multiplied by Gain(0dB=250mV)	2.5			dB
Sub FM Demodulation Det. Limitation	L_{f15}	4	Pin ㉔ Input (100mV$_{P-P}$) Pin ⑰ 3.5V	7			MHz
Main FM Demodulation Det. Sensitivity	S_{16}	5	Pin ㉑ Input (150mV$_{P-P}$) ⑰ 3.5V F_{11} is multiplied by Gain(0dB=250mV)	2.5			dB
Main FM Demodulation Det. Limitation	L_{f16}	5	Pin ㉑ Input (100mV$_{P-P}$) ⑰ 3.5V	7			MHz
Difference Det. Amp. Gain A	G_{11-1}	6	Pin ⑭ Input (100mV$_{P-P}$, 1MHz)	13.5		16.5	dB
Difference Det. Amp. Gain B	G_{11-2}	6	Pin ⑬ Input (100mV$_{P-P}$, 1MHz)	12		15	dB
Differrential+MIX Amp. Gain	G_{4-1}	7	Same as above	7		10	dB
MIX Amp. Ratio	G_{4-2}	7	Pin ⑫ Input (500mV$_{P-P}$, 1MHz)	−5.5		−2.5	dB
Line Noise Canceler Switch Changeover Level Difference	Δv_4	8	Pin ⑦ Control Pulse	−5		5	mV
Line Noise Canceler Switch Crosstalk	CT_4	9	500mV$_{P-P}$, 1MHz ④Output ratio of⑩and⑫			−40	dB
Line Noise Canceler Limiter Gain	G_7	10	Pin ⑨ Input (40mV$_{P-P}$, 1MHz)	15.5		19	dB
Line Noise Canceler Correlative Det. Sensitivity ON	S_6	11	Pin ⑨ Input (4MHz), 0dB=60mV$_{P-P}$	1.5		4.5	dB
Line Noise Canceler Correlative Det. Sensitivity OFF(Hysteresis)	ΔS_6	11	Pin ⑨ Input (4MHz), 0dB=60mV$_{P-P}$	−4		−0.1	dB
Picture Control Gain	G_1	12	Pin ③ Input (250mV$_{P-P}$, 1MHz) Output ratio of Pin②0V and 2.5V	−1.5		0.5	dB
Picture Control Frequency Characteristics A	f_{1-1}	12	Pin ③ Input (250mV$_{P-P}$, 1MHz)			−3	dB
Picture Control Frequency Characteristics B	f_{1-2}	12	Pin ③ Input (250mV$_{P-P}$, 1MHz) Output ratio of Pin②5V and 2.5V	5			dB

Note : Operating Supply Voltage Range : $V_{CC(opr)}$=4.5~5.5V

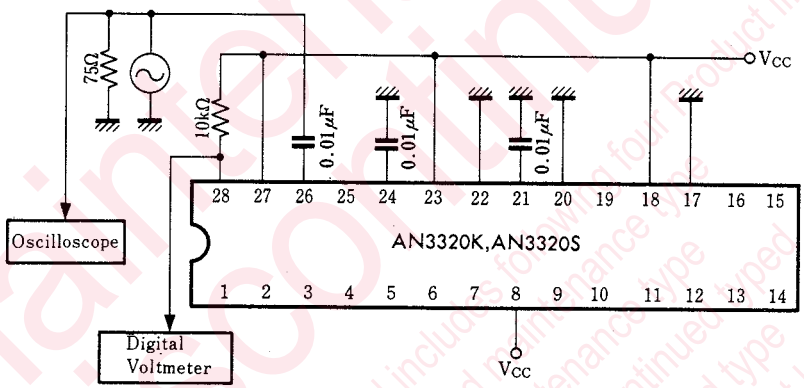
Test Circuit 1 (I_{23})



Test Cirucit 2 (G_{25})

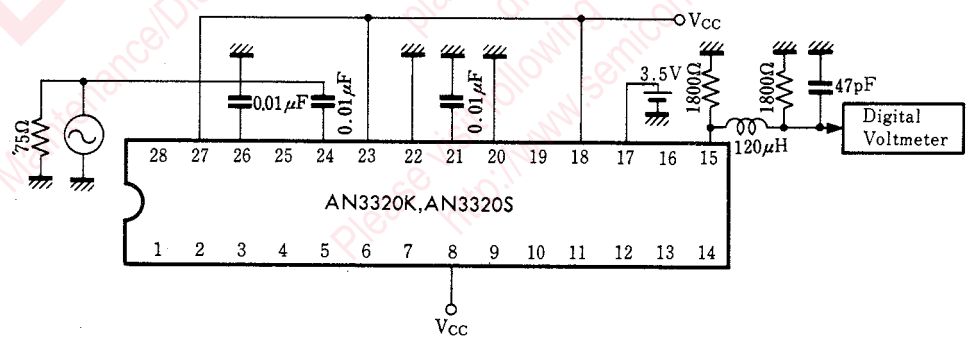


Test Circuit 3 (S_{28}, ΔS_{28})



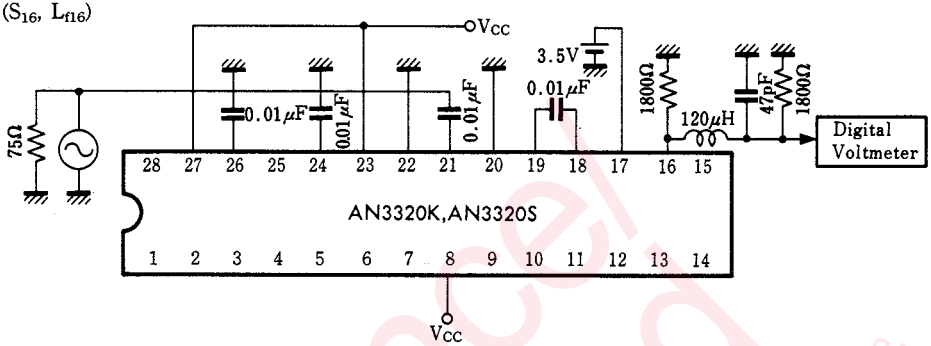
- S_{28-1} : Input level when Pin 28 output goes to Low
- S_{28-2} : Difference between input level and S_{28-1} when Pin 28 output goes to High

Test Circuit 4 (S_{15}, L_{f15})



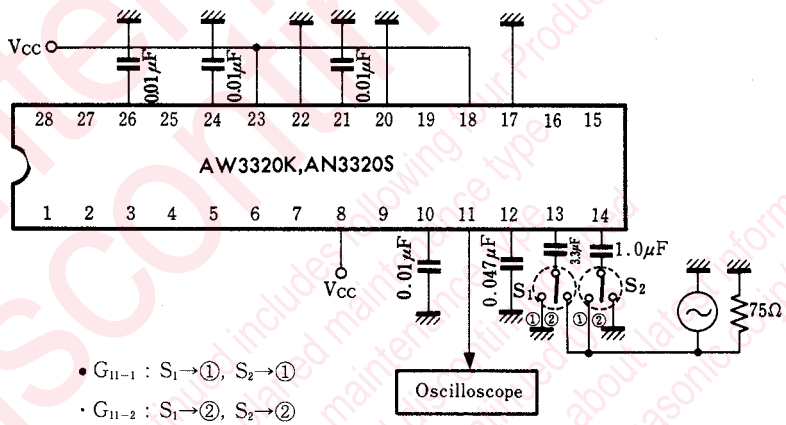
- S_{15} : Pin ⑮ output difference of input frequency 3.5MHz and 4.5MHz for Pin ㉔ is multiplied by F_{11} differential + Mix. Amp. gain.
- L_{f15} : Pin ㉔ input frequency when Pin ⑮ output changes

Test Circuit 5 (S_{16}, L_{f16})



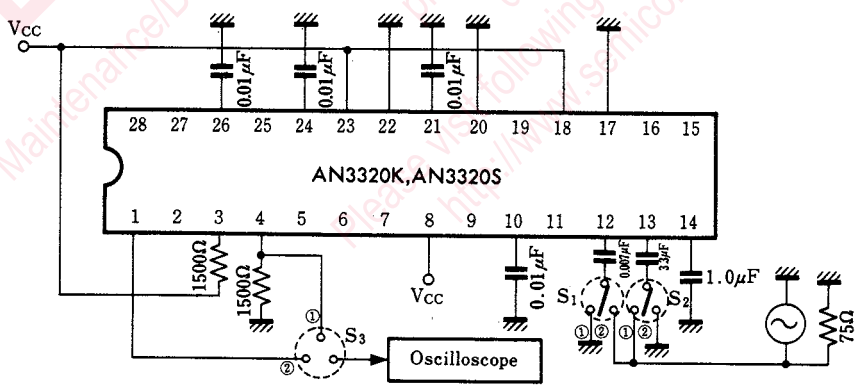
- S_{16} : Pin ⑯ output difference of input frequency 3.5MHz and 4.5MHz for Pin ㉖ is multiplied by F_{11} differential + Mix. Amp. gain.
- L_{f16} : Pin ㉑ input frequency when Pin ⑯ output changes

Test Circuit 6 ($G_{11\text{-}1}$, $G_{11\text{-}2}$)



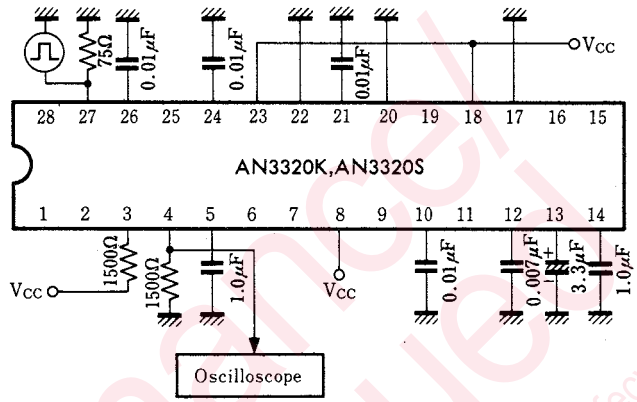
- G_{11-1} : $S_1 \rightarrow ①$, $S_2 \rightarrow ①$
- G_{11-2} : $S_1 \rightarrow ②$, $S_2 \rightarrow ②$

Test Cirucit 7 ($G_{4\text{-}1}$, $G_{4\text{-}2}$)

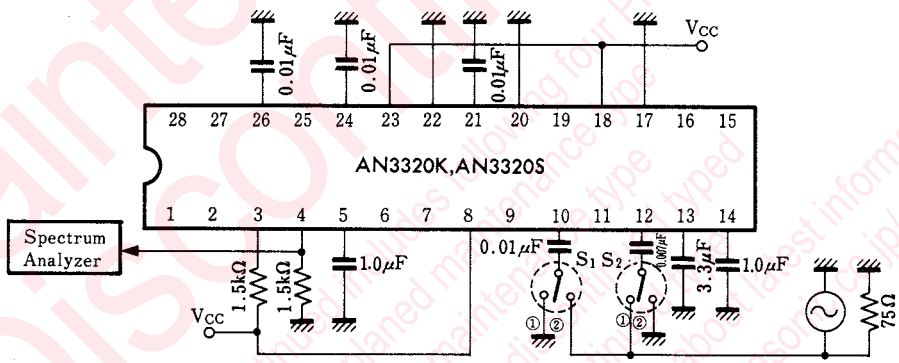


- G_{4-1} : $S_1 \rightarrow ①$, $S_2 \rightarrow ①$, $S_3 \rightarrow ②$
- G_{4-2} : $S_1 \rightarrow ②$, $S_2 \rightarrow ②$, $S_3 \rightarrow ①$

Test Circuit 8 (Δv_4)

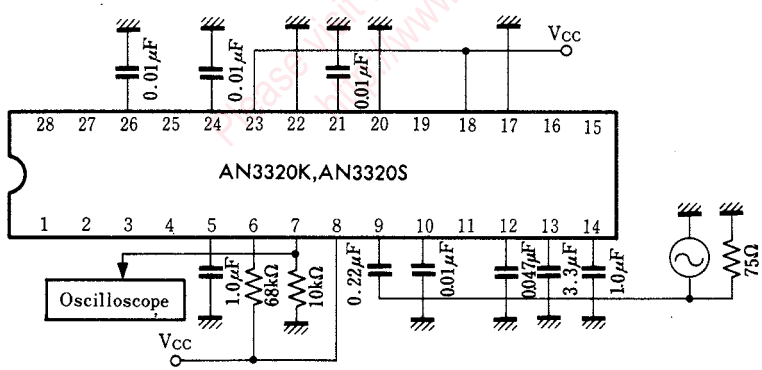


Test Circuit 9 (CT_4)

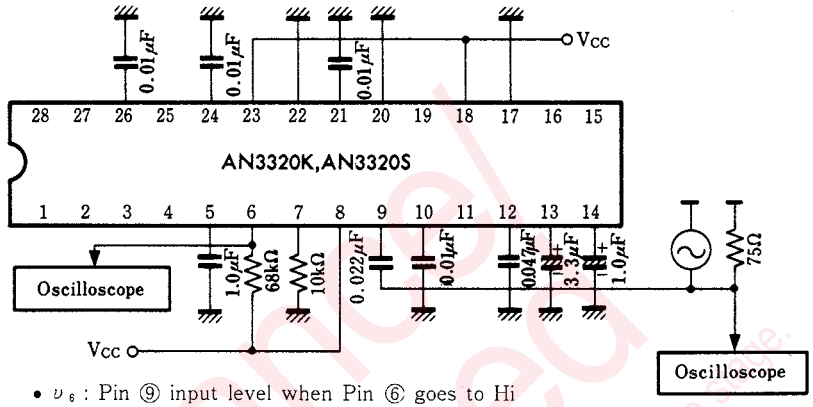


• CT_4: Pin ④ output for Pin ⑫ and element ratio for Pin ⑩ input corresponding to element

Test Circuit 10 (G_7)

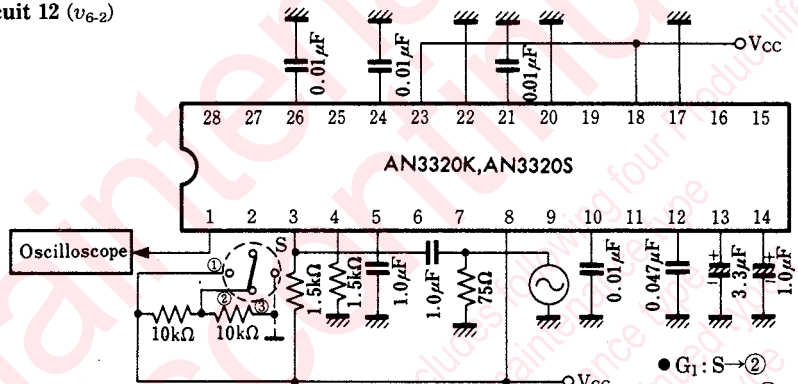


Test Circuit 11 ($v_{6\text{-}1}$, $v_{6\text{-}2}$)



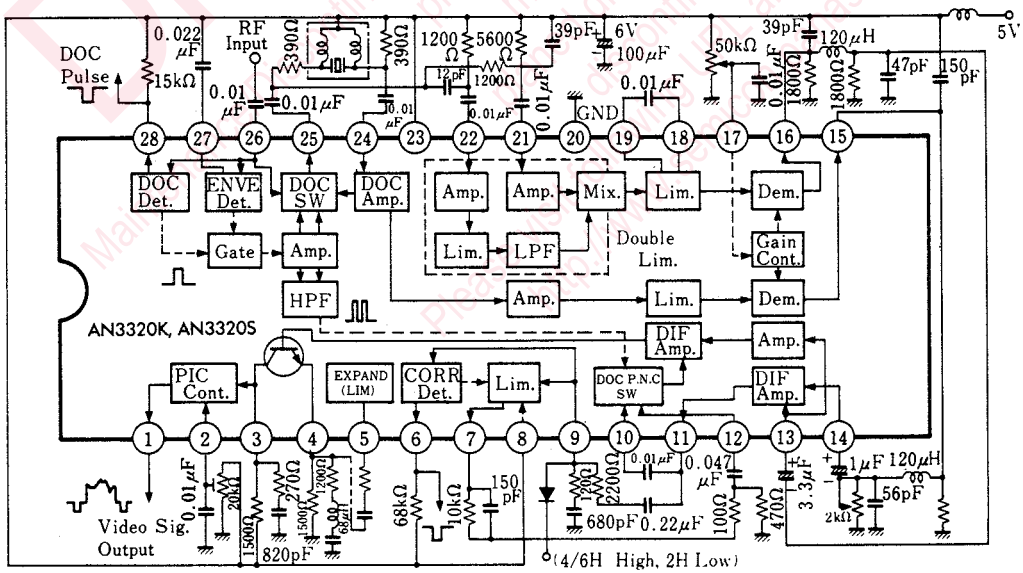
- v_6 : Pin ⑨ input level when Pin ⑥ goes to Hi
- Δv_6:Difference between input level when changed to L0 and v_6

Test Circuit 12 ($v_{6\text{-}2}$)



- G_1 : S→②
- $f_{1\text{-}1}$: S→③
- $f_{1\text{-}2}$: S→①

■ Application Circuit



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Video Output	15	DEM(1H DL)Output
2	Picture Control	16	DEM Output
3	De-emphasis	17	DEM Gain Control
4	Peaking	18	LIM
5	Extension	19	LIM
6	Relative Detecting Pulse Output	20	GND
7	Line N.C. LIM. Output	21	Double LIM LPF Input
8	To Except Rec V_{cc}	22	Double LIM HPF Input
9	Line N.C. LIM. Input	23	V_{cc}
10	Diff. Sig. Input	24	1H Delay RF Input
11	Diff. Sig. Output	25	RF Output
12	Limited Sig. Input	26	RF Input
13	Video Input	27	Envelop DET
14	Video(1H DL)Input	28	DOC Pulse Output

Notes for Use

1. Pin ⑧ shall be always used in connection with Pin ㉓
2. Power supply to be supplied to the variable resistor added to Pins ② and ⑰ shall be used the same as that supplied to this integrated circuit.
3. Since deterioration or destoroy of characteristics due to flow of overcurrent caused by reverse current, careful attention should be taken to handling.

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